A Whirlwind tour through PDPs

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Whirlwind I

- mid-40s Project Whirlwind. use computers for air defense
- 1947: digital computer Whirlwind I designed at MIT. Jay Forrester, Robert Everett
- Goals: fast, real time, interactive
- ~1950: WWI operational
- 16 bit words
- Instructions: 5 bit opcode. 11 bit address (2k)
- Memory: cathode ray tubes (not Williams tubes)
- Forrester invents core memory for WWI

Whirlwind I Peripherals

- Paper tape
- Scope
- Flexowriter
- Magnetic tape
- Drum
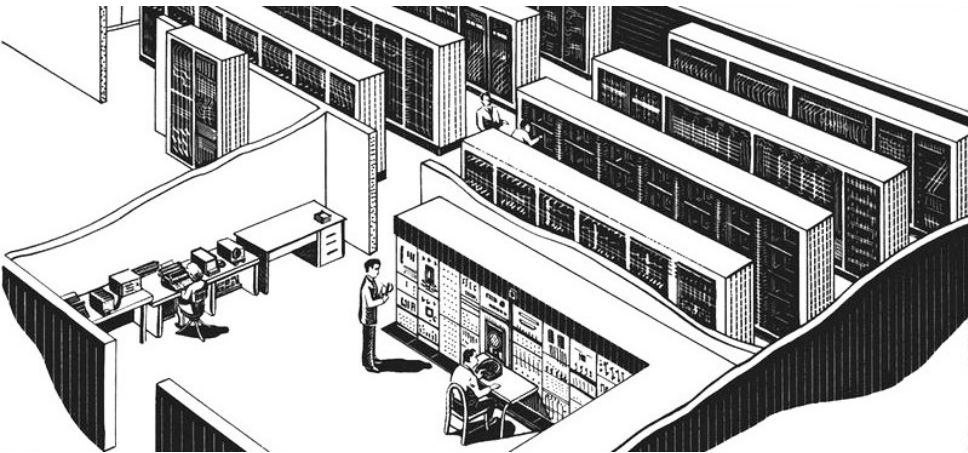
Whirlwind II

- WWII bigger successor to WWI. Named AN/FSQ-7 for SAGE
- Try out new ideas in a smaller machine: WWI½ $\rightarrow$ WWIA $\rightarrow$ Memory Test Computer

- Various design proposals
- Very similar to WWI
- Final design ca. 1952/53
- People involved: Ken Olsen, Wesley Clark, Harlan Anderson et al.

TX-0

- Ken Olsen and Wes Clark want to build a transistorized computer
- First proposed TX-1 too ambitious
- TX-0 simpler as proof of concept
- Built in 1955-56
- 18 bit words
- Instructions: 2 bit opcode. 16 bit address (64k)
- Moved to Cambridge in 1958 with 4k
- TX-2 much bigger (36 bits)

Digital Equipment Corporation

- Founded in 1957 by Ken Olsen, Harlan Anderson, Stan Olsen
- Bring simple fast interactive machines to the market that can be used to build systems
- Lab Modules
- System Modules
- Programmed Data Processor (PDP)

PDP-1

- Built in 1959 by Ben Gurley
- 18 bit words
- Instructions: 5 bit opcode. Indirection. 12 bit address (4k)
- ca. 50 sold

PDP-2 and PDP-3

- PDP-2: 24 bit PDP-1, but never built
- PDP-3: 36 bit PDP-1, but never built by DEC
- Indexing

PDP-4

- Designed by Gordon Bell as simpler and cheaper PDP-1
- 18 bit words
- Instructions: 4 bit opcode. Indirection. 13 bit address (8k)
- ca. 50 sold

PDP-5

- Designed by Gordon Bell as even smaller PDP-4
- The canonical minicomputer
- 12 bit words
- Instructions: 3 bit opcode. Indirection. 8 bit address
- 8 bit to 12 bit addressing scheme by Alan Kotok
- Very successful

PDP-6

- Designed by Gordon Bell with input from MIT hackers
- Big, timesharing computer
- 36 bit words
- 18 bit address (256k)
- 16 Accumulators/Index registers
- Indirection, Indexing
- Not very successful